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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,008	09/28/2001	Joerg Vollrath	INTECH 3.0-013	5624

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,008	VOLLRATH ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,13-16,21-23,25,26 and 33-36* is/are rejected.

7)☐ Claim(s) *4, 7-12, 17-20, 24, 27-32, and 37-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/06/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 03/06/02 in application 09/967,008.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in

order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3, 5-6, 13-16, 21-23, 25-26, and 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wheelus et al. (U.S. Patent 5,677,917 hereafter referred to as Wheelus) in view of Sugimura et al. (U.S. Patent 4,653,051 hereafter referred to as Sugimura).

As per claim 1:

Wheelus substantially teach the invention. Wheelus teaches:

- A memory [abstract, fig. 1],

comprising:

- a memory array having a plurality of storage elements [abstract, fig. 1, col. 2, line 7];

- a plurality of replacement storage elements [col. 2, lines 16-20];

- a plurality of address fuse units, each having a plurality of fusible links [col. 3, line 37] and being operable to store a replacement address, each replacement address identifying one of the storage elements of the memory array to be replaced by an associated one of the

replacement storage elements and forming a respective 2.sup.m bit row or 2.sup.n bit column of a fuse array [col. 3, lines 35-49 and col. 8, lines 48-50];

- a vector generator operable to produce a 2.sup.n bit row vector based on the rows of the fuse array and to produce a 2.sup.m bit column vector based on the columns of the fuse array [col. 6, lines 26-50].

Wheelus does not explicitly teach:

- a compression unit operable to produce a row checksum from the row vector and to produce a column checksum from the column vector.

However, Wheelus does disclose capability of:

- An integrated circuit memory using fusible links in a scan chain [abstract, fig. 6, col.1, lines 5-7] comprising capability of:

- memory array redundancy, memory testing, memory debugging, memory repairing (i.e., checksum used within implicitly) [col. 1, lines 23-40 and col. 6, lines 65 through col. 7, lines 8].

In addition, Sugimura explicitly teaches:

- An apparatus for detecting and correcting errors [abstract, fig. 1, col. 1, lines 7-11];

comprising:

- row and column checksum capability performed via XOR logic to detecting and correcting error [col. 1, line 60 through col. 2, line 2, and col. 11, line 36 through col. 12, line 17].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply the row and column checksum capability performed via XOR logic to detecting and correcting error as taught by Sugimura in conjunction with the integrated circuit memory using fusible links in a scan chain as disclosed by Wheelus in order to enhance the memory, more specifically to ensuring the memory location error detection, correction, and replacement in proper and efficient manner. One of ordinary skill in the art would have been motivated to do so to improve the memory location, memory access, memory availability and memory integrity.

As per claims 2-3:

Wheelus substantially teach the invention. Wheelus teaches:

- A memory [abstract, fig. 1],

- the vector generator is operable to produce each bit of the row vector by determining a logic combination of the 2.sup.m bits of a corresponding one of the rows of the fuse array [col. 6, lines 26-5];

-the vector generator is operable to produce each bit of the column vector by determining a logic combination of the 2.sup.n bits of a corresponding one of the columns of the fuse array [col. 6, lines 26-50];

-the memory of claim 2, wherein: the vector generator is operable to produce each bit of the row vector by determining an XOR of adjacent ones of the 2.sup.m bits of the corresponding row of the fuse array ***(i.e., fusible in a scan chain)*** [col. 2, lines 37-52 and col. 6, lines 26-5];

- the vector generator is operable to produce each bit of the column vector by determining an XOR of adjacent ones of the 2.sup.n bits of the corresponding column of the fuse array ***(i.e., fusible in a scan chain)*** [col. 2, lines 37-52 and col. 6, lines 26-5].

As per claims 5-6:

Wheelus further teaches:

- fusible link in a scan chain [col. 1, lines 6-7];

- a memory array having a plurality of storage elements [abstract, fig. 1, col. 2, line 7];

- a plurality of replacement storage elements [col. 2, lines 16-20];

- a plurality of address fuse units, each having a plurality of fusible links [col. 3, line 37].

Wheelus does not explicitly teach:

- a compression unit operable to produce a row checksum from the row vector and to produce a column checksum from the column vector by determining a logic combination or an XOR combination.

However, Wheelus does disclose capability of:

- An integrated circuit memory using fusible links in a scan chain [abstract, fig. 6, col.1, lines 5-7] comprising capability of:

- memory array redundancy, memory testing, memory debugging, memory repairing (i.e., checksum used within implicitly) [col. 1, lines 23-40 and col. 6, lines 65 through col. 7, lines 8].

In addition, Sugimura explicitly teaches:

- An apparatus for detecting and correcting errors [abstract, fig. 1, col. 1, lines 7-11];

comprising:

- row and column checksum capability performed via XOR logic to detecting and correcting error [col. 1, line 60 through col. 2, line 2, and col. 11, line 36 through col. 12, line 17].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply the row and column checksum capability performed via XOR logic to detecting and correcting error as taught by Sugimura in conjunction with the integrated circuit memory using fusible links in a scan chain as disclosed by Wheelus in order to enhance the memory, more specifically to ensuring the memory location error detection, correction, and replacement in proper and efficient manner set forth as described in claim 1, **supra**.

As per claims 13-16:

Wheelus further teaches:

- fusible link in a scan chain [col. 1, lines 6-7];
- error detector for comparison [col. 6, lines 38-50];
- replacement addresses faulty [col. 2, lines 16-20].

Wheelus does not explicitly teach:

- a row and a column checksum comparison.

Sugimura explicitly teaches:

- An apparatus for detecting and correcting errors [abstract, fig. 1, col. 1, lines 7-11];

comprising:

- row and column checksum comparison from different data for its resultant checksum in supporting the error detection and correction [col. 5, lines 40-65].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to apply - row and column checksum comparison from different data for its resultant checksum in supporting the error detection and correction as taught by Sugimura in conjunction with the integrated circuit memory using fusible links in a scan chain as disclosed by Wheelus in supporting the memory failure replacement. One of ordinary skill in the art would have been motivated to do so to improve the memory location, such as, first, any error or failure occurred in memory can be identified, detected, corrected via data comparison/checking; and second, the checksum comparison and execution can operate

with a high reliability and flexibility environment which will correctly be fencing or preventing any illegal access to the memory.

As per claims 21-23, 25-26, and 33-36:

Due to the similarity of claims 21-23, 25-26, and 33-36 to claims 1-3, 5-6, 13-16, except for a method for employing a checksum for addresses of replaced storage elements comprising steps of forming a fuse array, producing 2n bit row vector, producing 2m bit column vector, producing a row checksum, producing a column checksum, etc… instead of a memory for employing a checksum for addresses of replaced storage elements comprising capabilities of forming a fuse array, producing 2n bit row vector, producing 2m bit column vector, producing a row checksum, producing a column checksum, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-3, 5-6, 13-16. **In addition, all of the limitations have been noted in the rejection as per claims** 1-3, 5-6, 13-16.

Allowable Subject Matter

5. Claims 4, 7-12, 17-20, 24, 27-32, and 37-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408 **[NOTE: After approximately October 15, 2004, I can be reached at the new number (571) 272-3660].** The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER
ART UNIT 2114

DML
8/19/04